

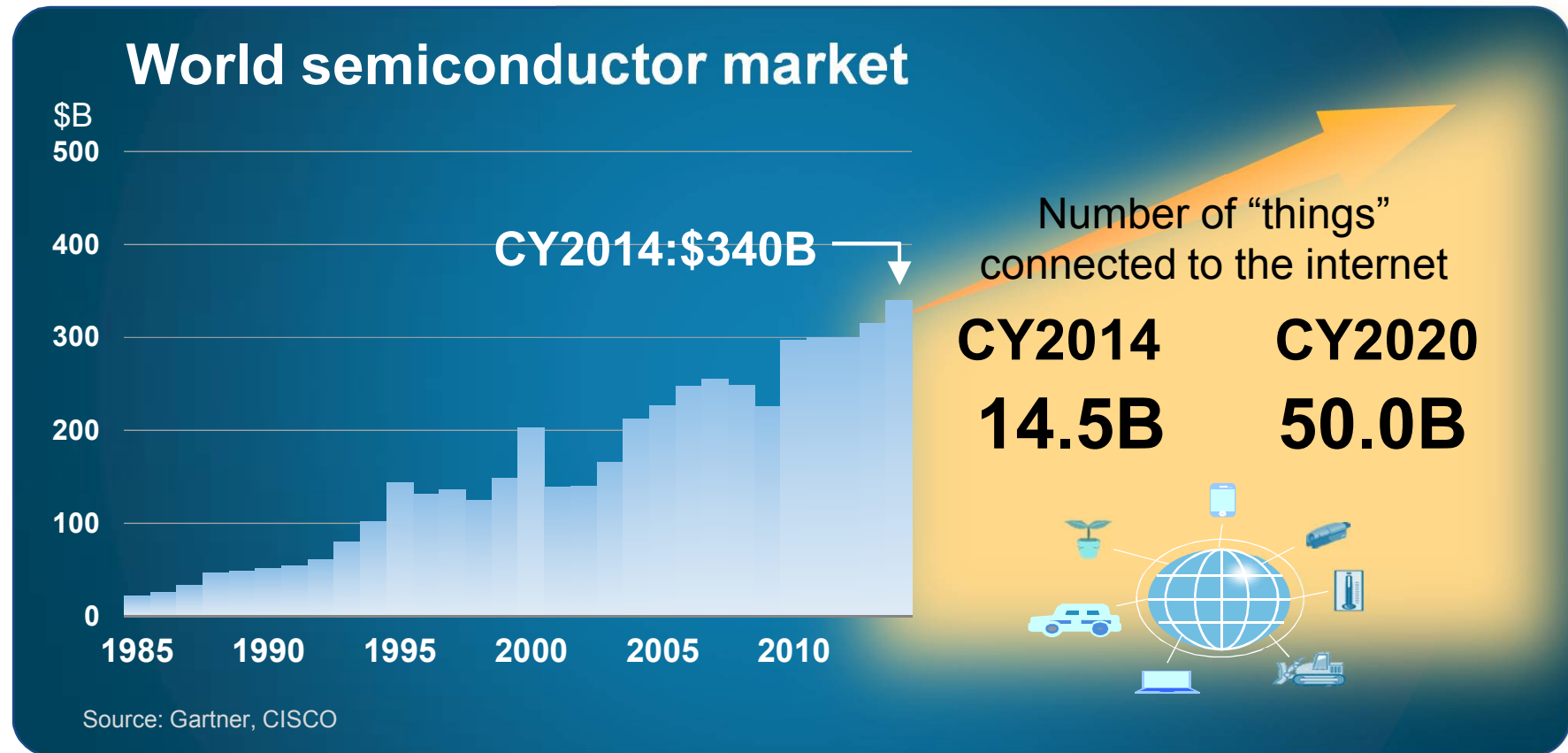
Creating a New TEL: Key Initiatives

Tetsuro Higashi
Representative Director, President & CEO
July 10, 2015



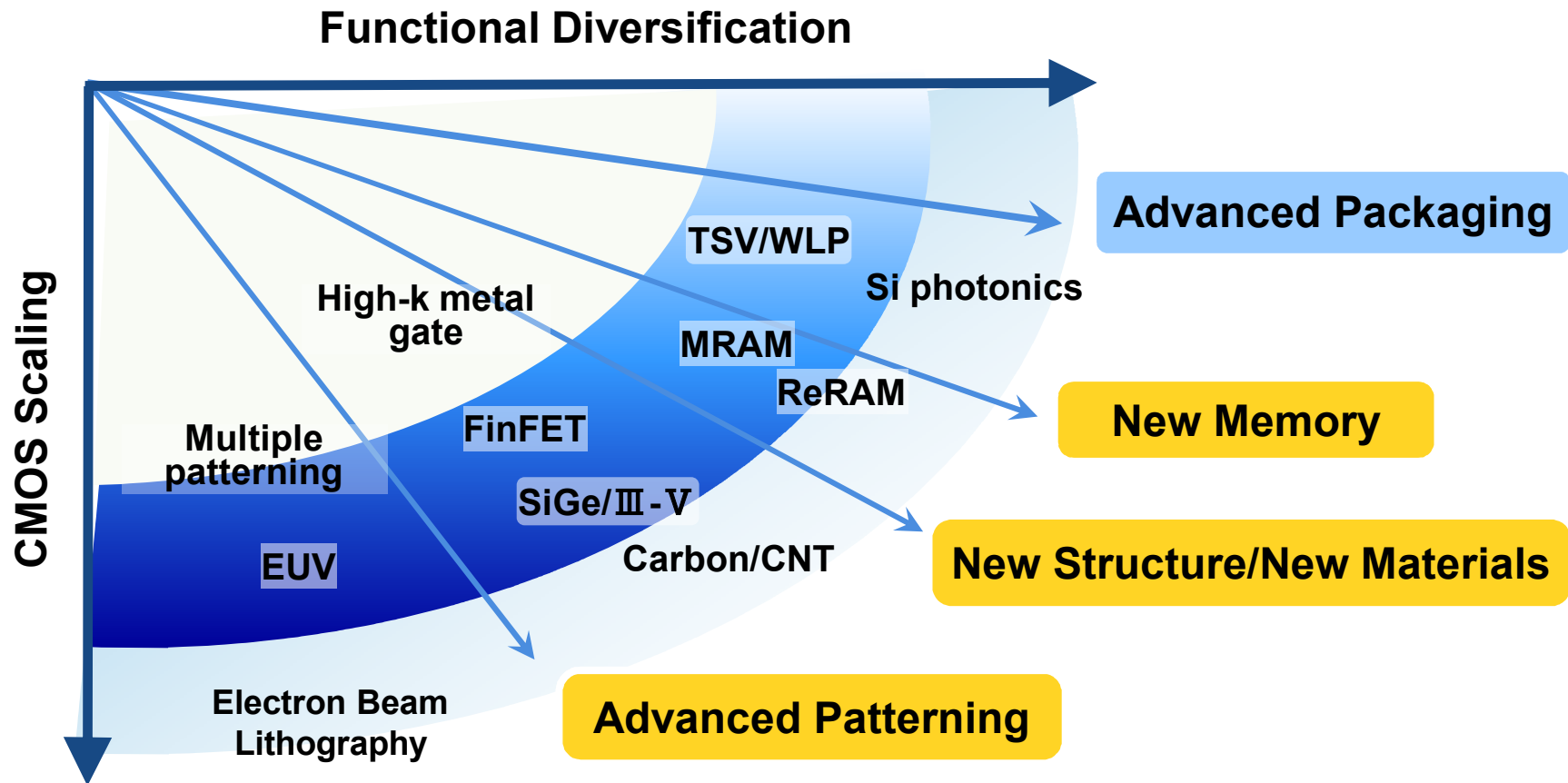
TOKYO ELECTRON

Changing Market Environment: The IoT Era is Coming



**Paradigm shift to IoT will lead to increased applications
and expand the semiconductor market**

Direction of Technological Innovations



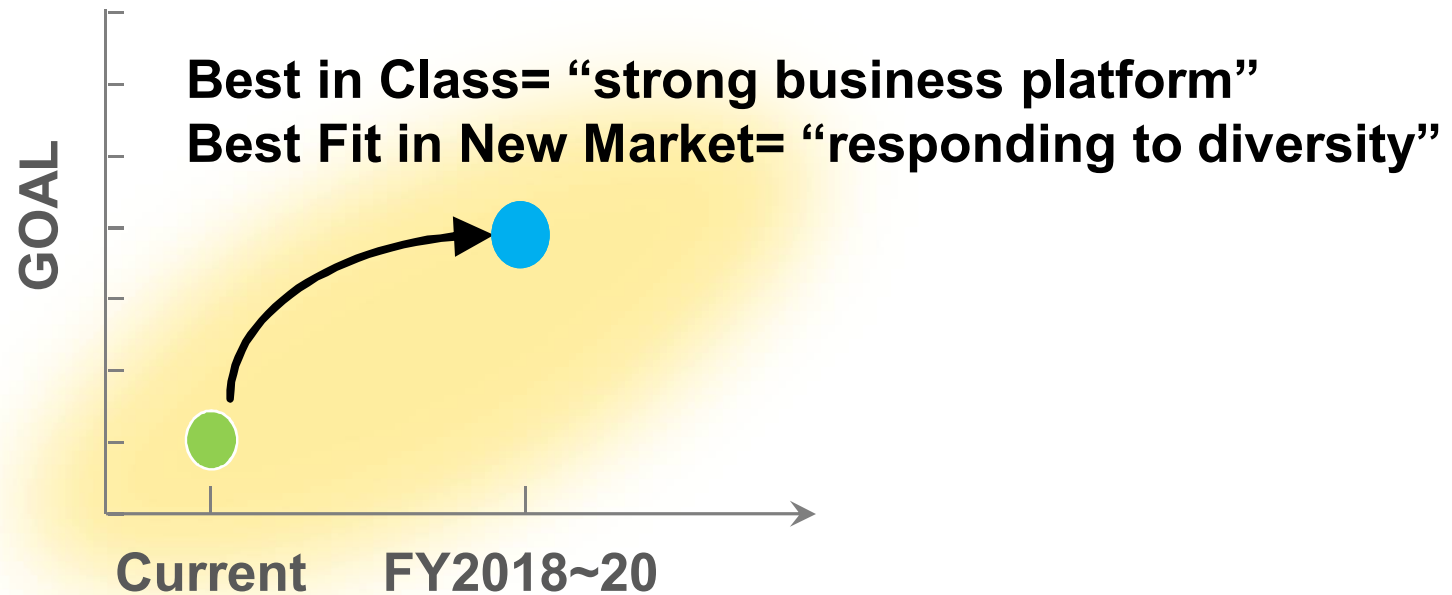
Evolution of semiconductors involves new, extensive technologies

Vision

A real global company generating high added-value and profits to Semiconductor and FPD industries through innovative technologies and groundbreaking solutions with integrated diverse technologies

Medium-term Business Direction

1. Best in Class
2. Best Fit in New Market

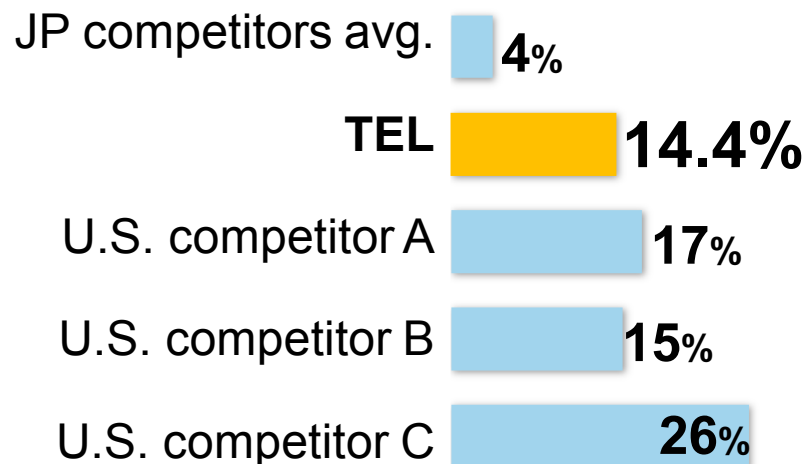


Strengthen platform and response capability to support further major advances

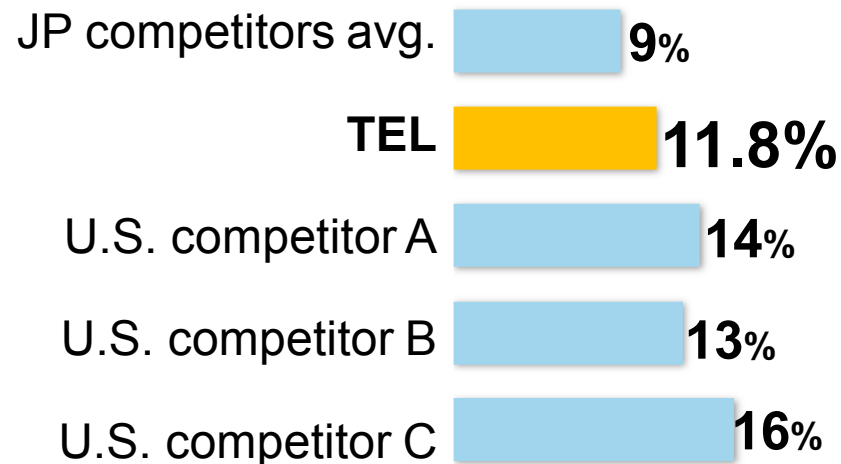
“Best in Class”

Benchmarks (Most Recent Fiscal Year)

Operating margin



ROE



**TEL still positioned behind U.S. peers
despite some improvement**

“Best in Class”

New Financial Model

Wafer Fab Equipment Market size	\$30B	\$37B
Sales	¥720B	¥900B
Operating margin	20%	25%
ROE	15%	20%

Aiming for global-level results

The semiconductor production process can be divided into two sequential sub-processes referred to as front-end (wafer fabrication) and back-end (assembly and test) production. WFE (wafer fabrication equipment) is used in the front-end production process.

“Best Fit in New Market”

Global Growth Strategy

**Changing market
environment**
IoT era

**Changing customer
needs**
Diversification of
differentiated technology

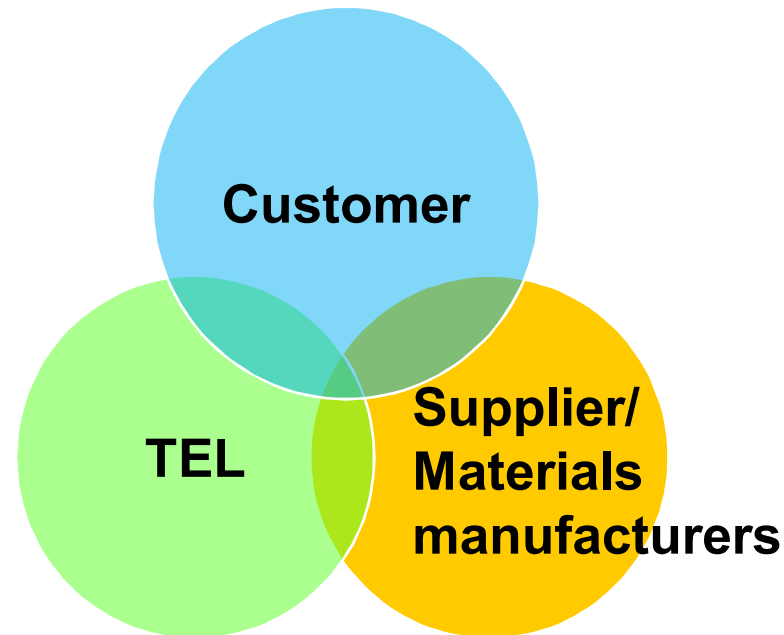


Approaches to diversification

- Grasp customers' true needs for **differentiation and customization**
- Provide solutions **bringing our technological strengths all together, extensively and swiftly**

“Best Fit in New Market”

Global Growth Strategy



Fully utilize TEL’s corporate DNA—our track record of creating strong relationships of mutual trust, and work closely with customers to overcome tough technological challenges

“Best Fit in New Market”

Transition to a New Structure

Key points of structural reform:

- **Created COO post**
- **CSS that enables swift business execution**
- **Appointed younger generation directors with broad knowledge**
- **Utilize global talent**

Become a company that identifies customers’ needs and surpasses their expectations

CSS: Corporate Senior Staff

Key Initiatives for Achieving Targets

- **Overwhelming differentiation in core businesses**
- **Shift to creating customer needs**
- **Reinforce foundation for realizing growth and technological innovation**
- **Improve efficiency of operations**
- **Utilize global talent**

New Corporate Logo

New Corporate Logo



TOKYO ELECTRON

- The square placed in the center of the logo signifies the high precision of TEL's technology. It also represents core technology, which is essential for the growth of industry and society.
- The new youthful, vibrant green represents a human element as well as environmental conservation, which is a key focus in TEL's business.
- The neat, polished, and universal shape represents TEL's absolute trust and presence, showing our organization's fairness.
- Global design which shows our company achieving global excellence.

Medium-term Management Plan

Toshiki Kawai

Representative Director, Senior Executive Vice President & COO

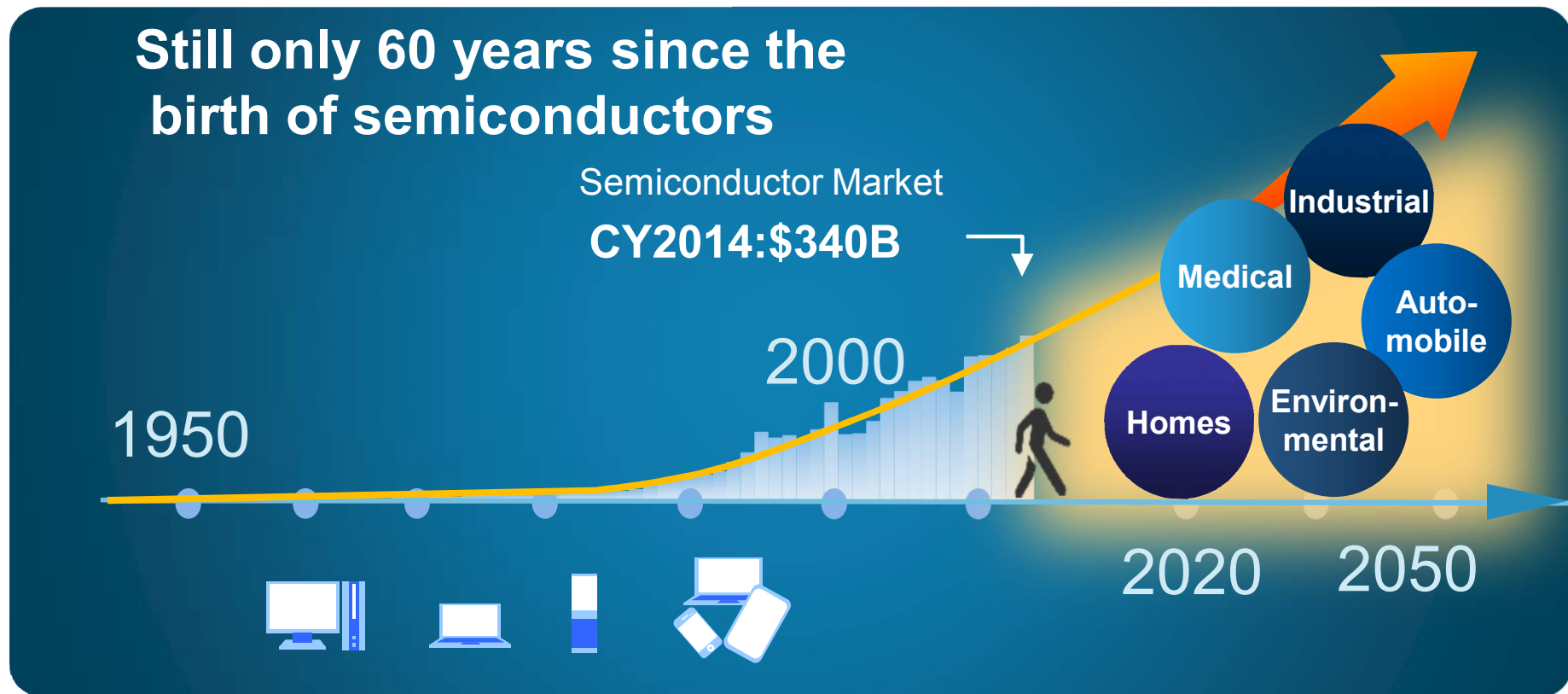
July 10, 2015



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Market Environment

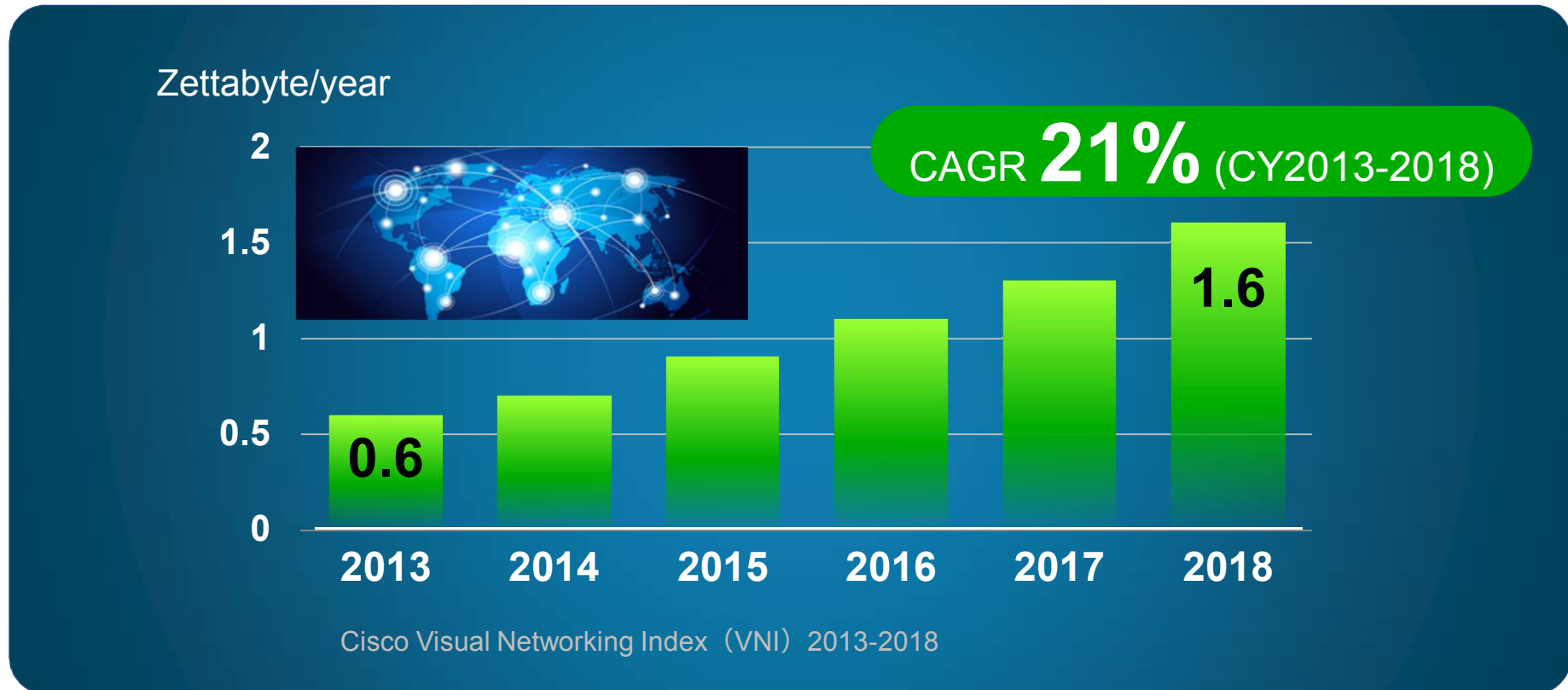
Network society



Semiconductors still only in the early stages

Market Environment

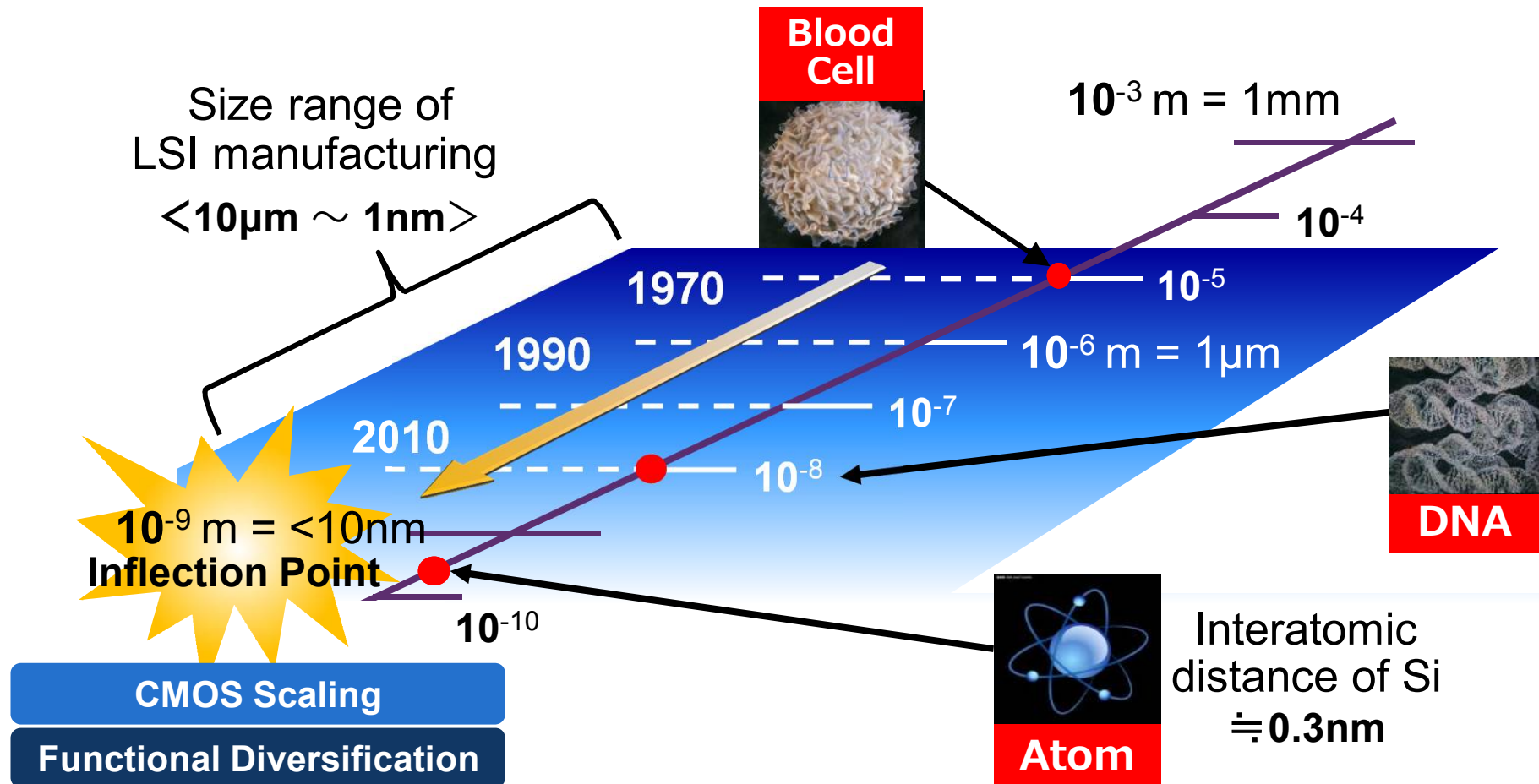
World IP traffic



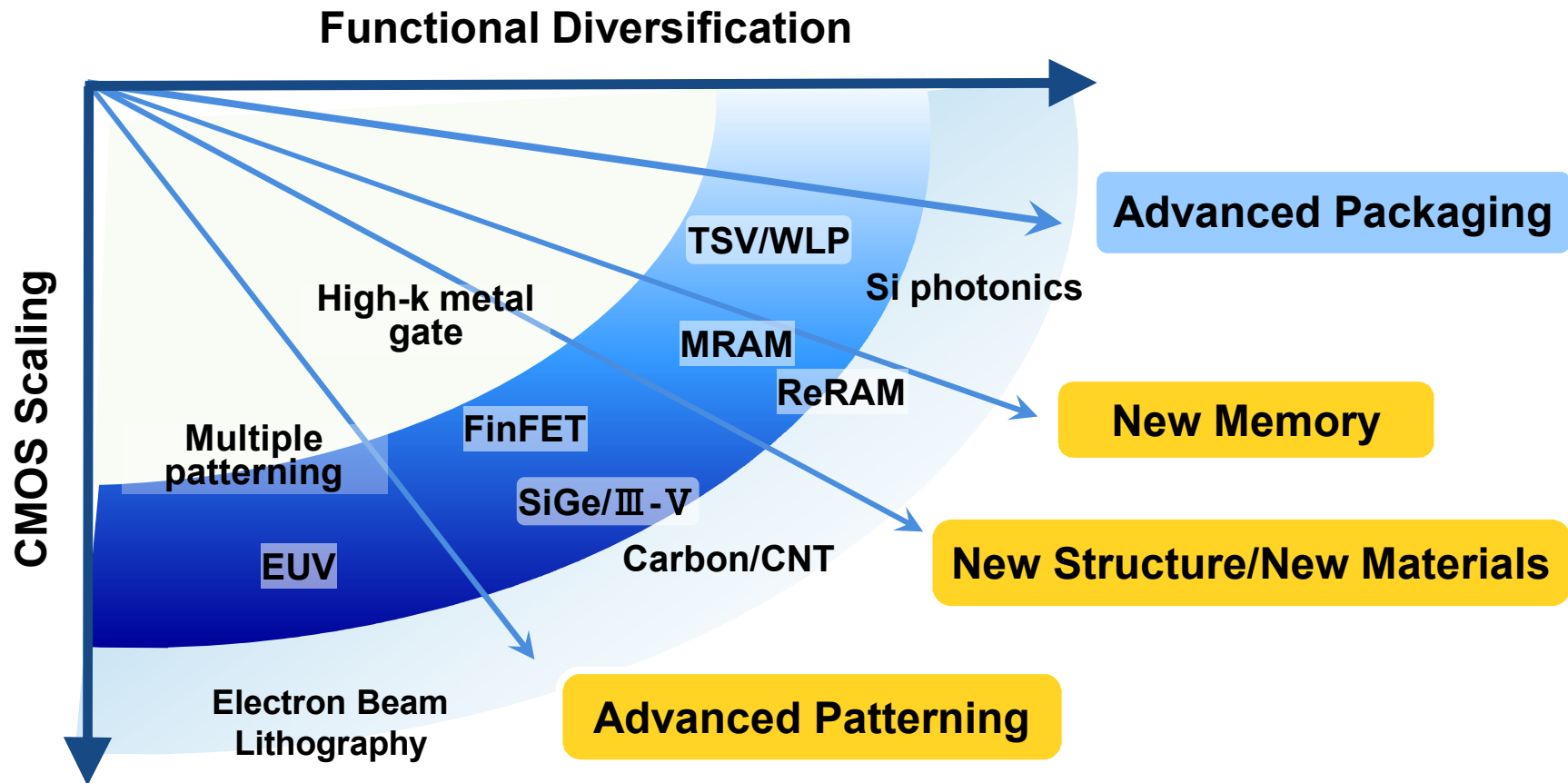
Data sent on networks will continue to increase explosively

Zettabyte: Unit indicating the magnitude of computer storage devices and digital data. 10^{21} bytes

Semiconductor Industry at an Inflection Point

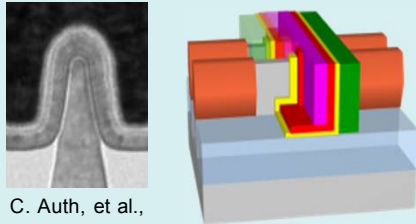
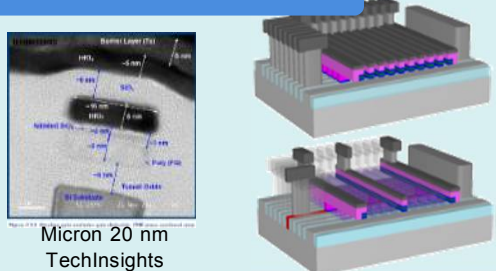
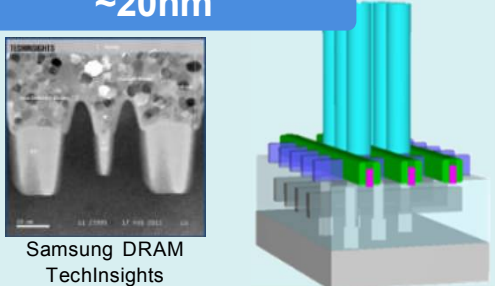
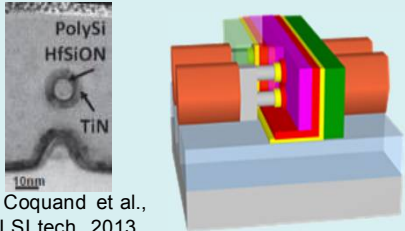
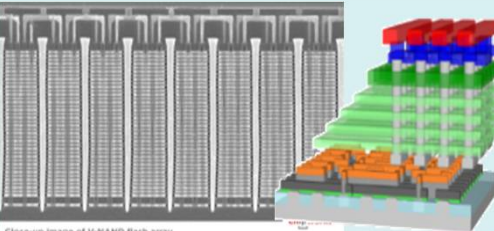
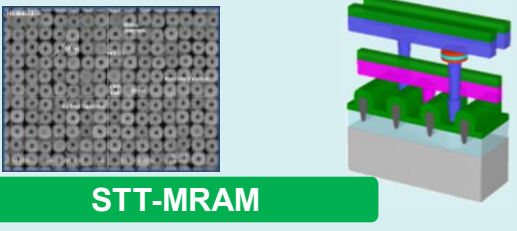


Direction of Technological Innovations



Evolution of semiconductors involves new, extensive technologies

Technological Trends: High-volume Manufacturing & Next-generation Devices

	Cutting-edge logic	Flash Memory	DRAM
High-volume manufacturing (present)	<p>16/14nm (2nd Gen. FinFET)</p>  <p>C. Auth, et al., VLSI tech. 2012</p>	<p>2D FG-NAND 15nm</p>  <p>Micron 20 nm TechInsights</p>	<p>~20nm</p>  <p>Samsung DRAM TechInsights</p>
Next generation (2018~)	<p>7nm (nanowire, new materials)</p>  <p>R. Coquand et al., VLSI tech. 2013</p>	<p>3D NAND 64 layer stacking</p>  <p>Close-up image of V-NAND flash array</p>	<p>Continuous 1x/1y scaling</p>  <p>STT-MRAM</p>
Technological inflection points	<p>Challenges: Speed and low power consumption</p> <ul style="list-style-type: none"> • Shift to 3D structure device (FinFET) • New structures (nanowire) • New materials 	<p>Challenge: Integration</p> <ul style="list-style-type: none"> • Shift to 3D layer stacking • Etching and deposition technology for high-aspect structure 	<p>Challenge: Capacitor capacity</p> <ul style="list-style-type: none"> • High-aspect etching • Shift to ALD for capacitor materials • Possibility of partial replacement with MRAM

Identify technological inflection points and provide solutions

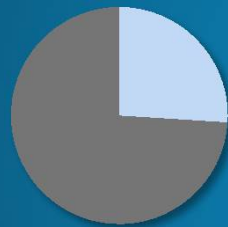
Our SPE Competitiveness

TEL product market share (CY2014)

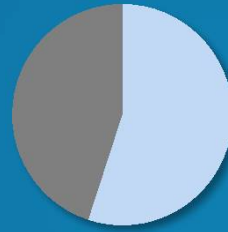
Overwhelming competitiveness



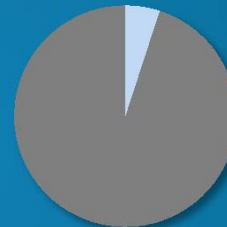
Coater/
developer



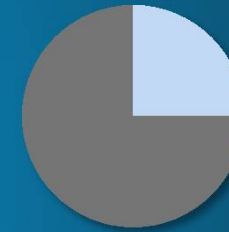
Etch



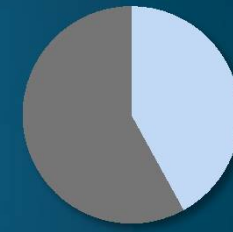
Thermal
processing



Single wafer
deposition



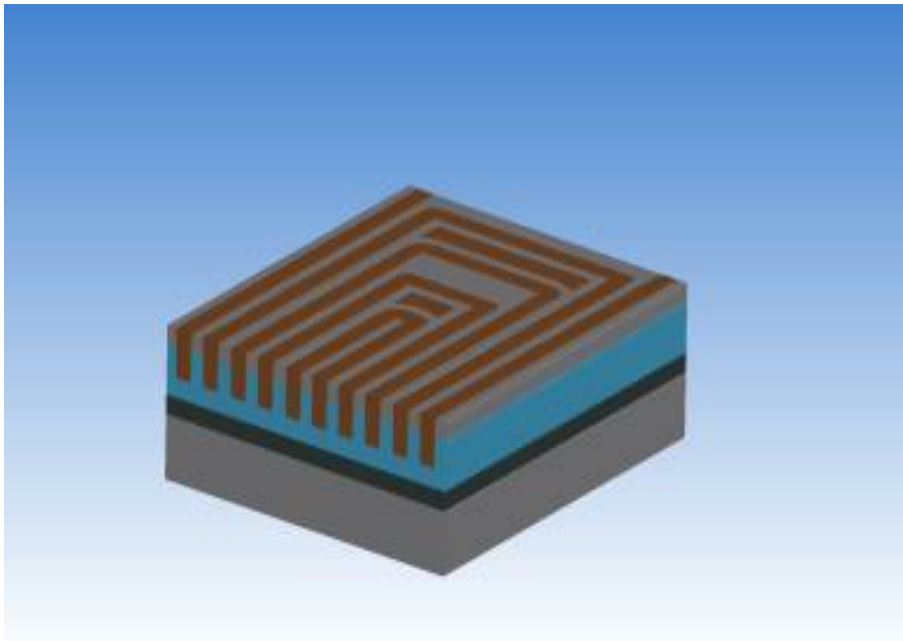
Cleaning



Wafer
prober

Source: Gartner

SPE Products: Broad Product Line Up in Patterning



Process Finished



Clean Track

LITHIUS Pro™ Z



ALD Film Deposition

*NT333™, Triase+™ EX-II™,
TELINDY PLUS™ IRad*



Dry Etch

Tactras™



CVD Film Deposition

Triase+™ CVD, TELINDY PLUS™



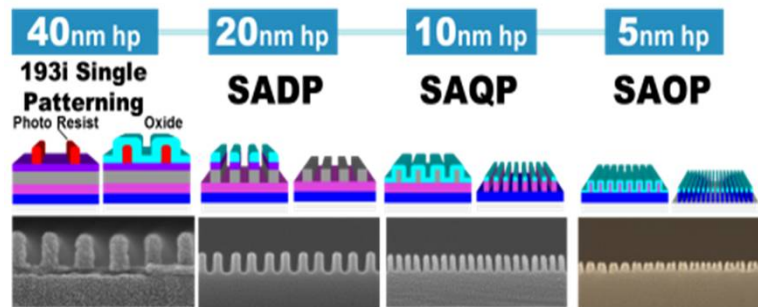
Wet Cleaning

CELLESTA™ -i

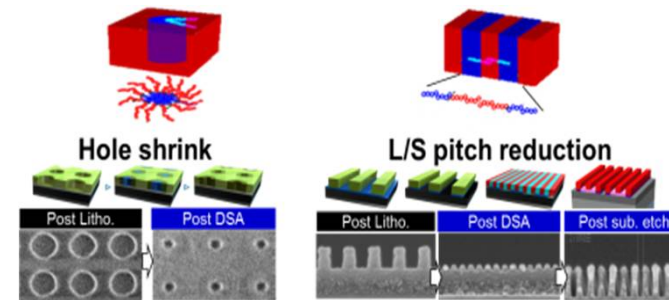
SPE Business Strategy: Strengthen Ability to Provide Technological Solutions in Patterning

“Patterning Solution Project”

Respond to customer needs for leading-edge technology by leveraging broad product line



Multiple patterning technology



DSA* technology
*Directed Self-Assembly

SPE Business Strategy: STT-MRAM Development



Gas cluster ion beam system



Single wafer cleaning system



Etch/CVD system



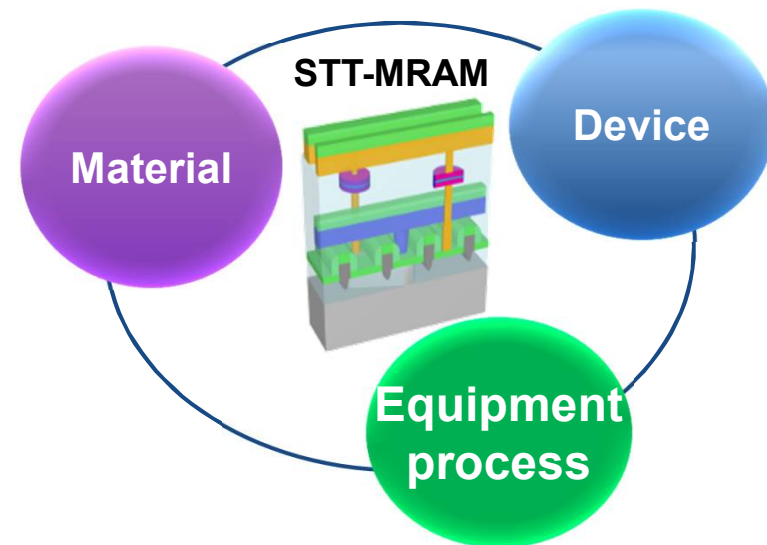
Magnetic annealing system



MTJ sputtering system

- **Strengthen development with customers, Tohoku University, and consortia**
- **Lead development for practical use**

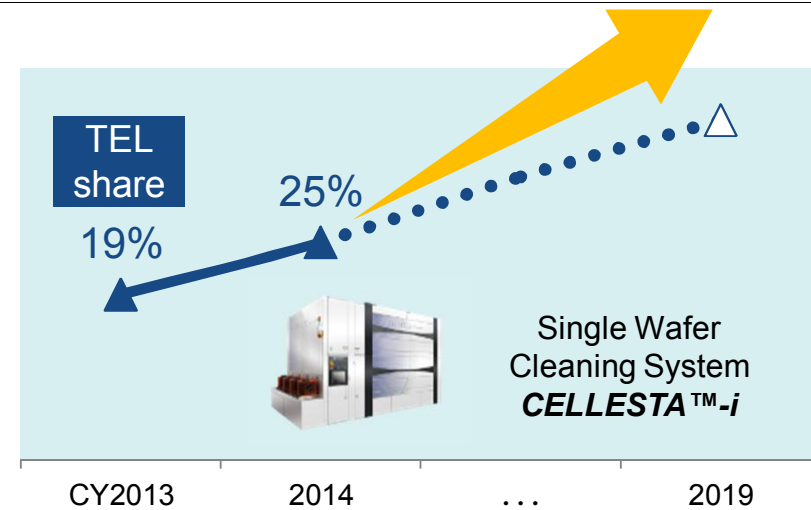
STT-MRAM: Spin Transfer Torque-Magnetoresistive Random Access Memory



SPE Business Strategy: Topics and Key Strategies by Equipment Category

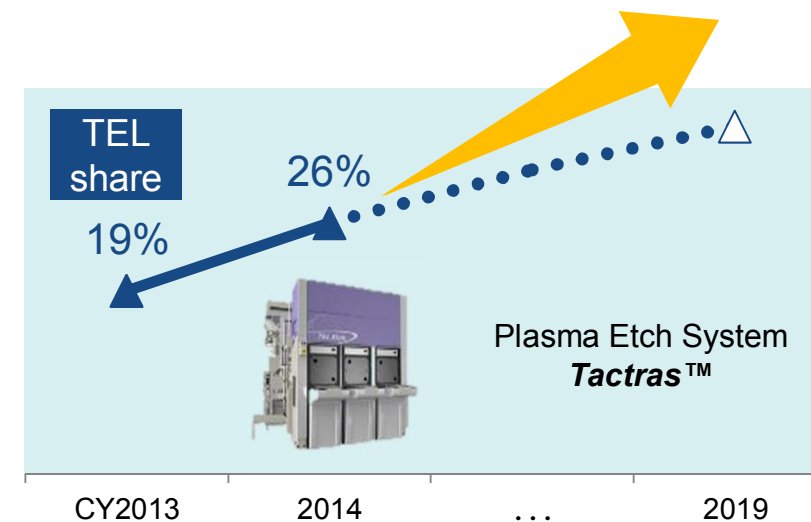
Cleaning system

- Highest ever market share in 2014
- Customer penetration in leading-edge HVM lines progressing as planned, with our proprietary technology
- Expand applications of single wafer cleaning and dry cleaning system and further increase market share



Etching system

- Doubled sales in 2014 YoY and increased market share
- Acquire POR in patterning and memory HARC processes, where growth expected



POR (Process of Record): Certification of equipment application in customer semiconductor manufacturing process
HARC: High Aspect Ratio Contact

Source : Gartner (market share in 2013 and 2014) and TEL estimate

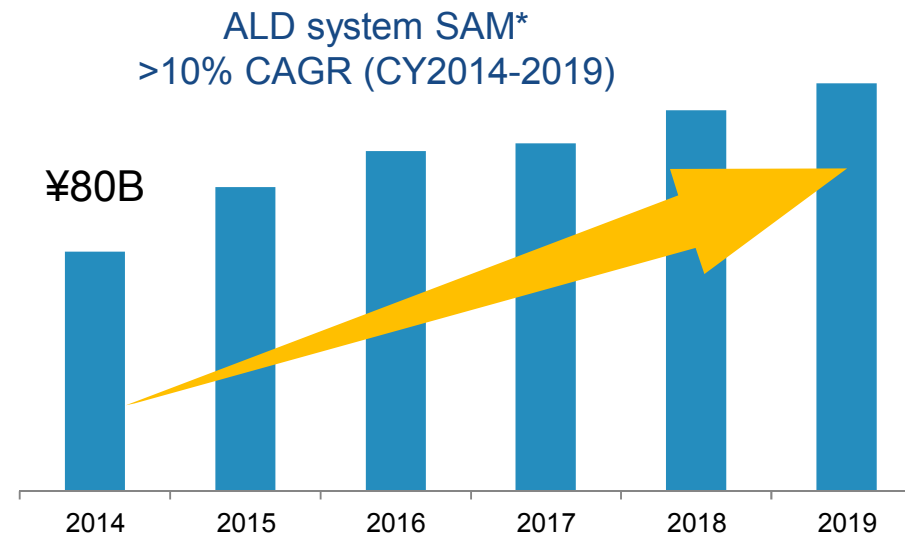
SPE Business Strategy: Topics and Key Strategies by Equipment Category

ALD system

- Respond to needs for high coverage and productivity required in miniaturization and 3D structure
- Expect to acquire POR and share in logic and memory with semi-batch ALD system NT333, which is differentiated by its high productivity and high-quality film



ALD system
NT333™



*SAM: Served Available Market

Source: TEL estimate

SPE Business Strategy: Strengthen Field Solutions Business

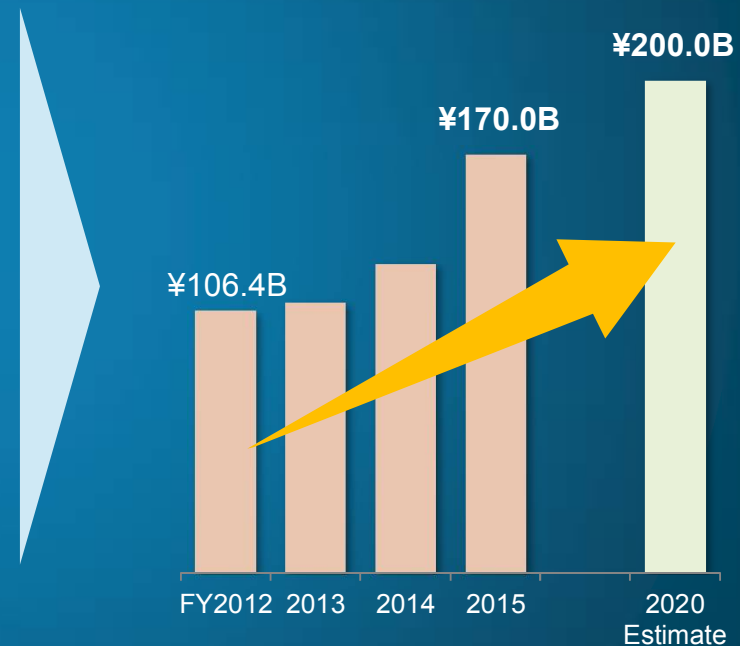
Expanding business opportunities

The IoT era will bring demand for diverse semiconductor technologies

Explosive growth of IP traffic = semiconductor growth

TEL's installed base
54,000 units

Support customer needs in existing production lines



Field solutions business sales are included in SPE and FPD segment sales.

Expand field solutions business opportunities in IoT era

SPE Business New Framework

New framework and executive structure to “Enhance our strengths”

- Enhance our core strength—the full trust of our customers
- Implemented account and region management structures
- Create value-added products leveraging the integration of the core technology and expertise of each BU
- Launched patterning solution project
- Maximize the strengths in value creation and efficiency of each plant and development site

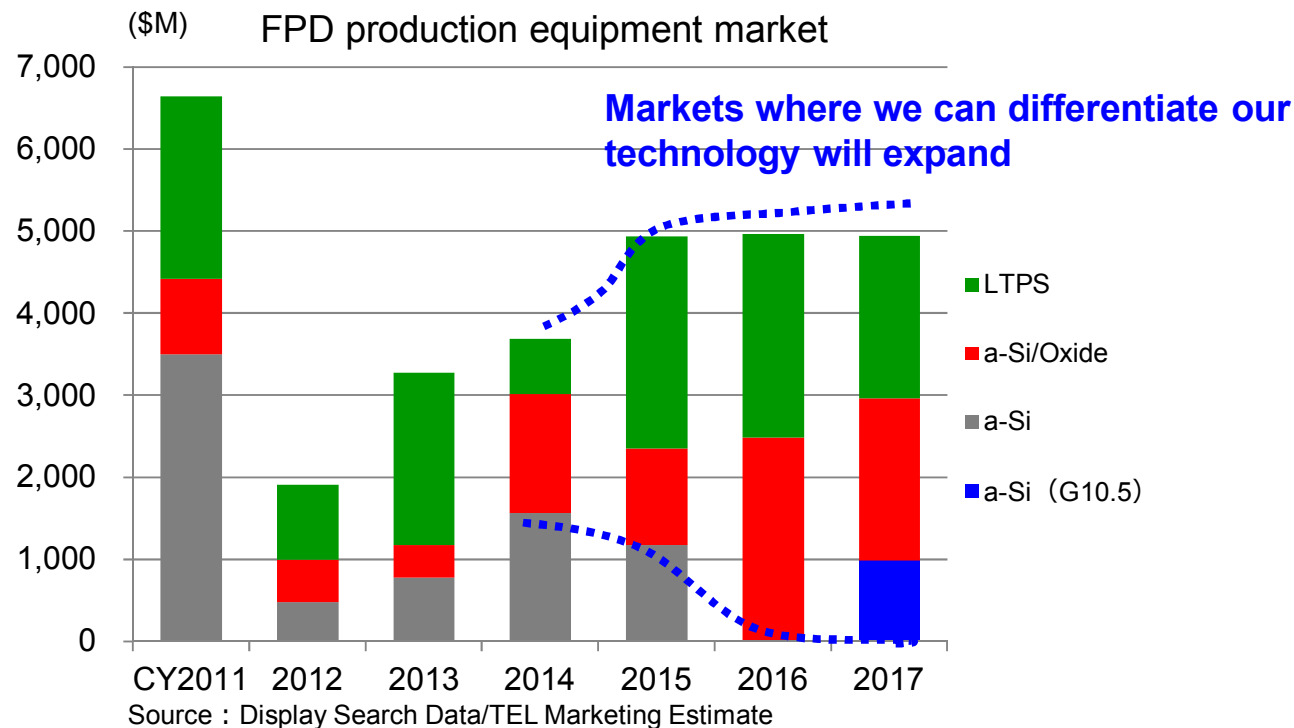
Global Field Division

**Business Promotion
Division**

**Development &
Manufacturing Division**

FPD Business Strategy

Shift to large-size panels, increased demand for high-resolution for smart phones. Introduced our differentiated ICP* etch systems in growing LTPS/metal oxide market



**Increase market share and profitability,
aim for 20% OPM**

* ICP : Inductively Coupled Plasma

Summary

Toward profitability and ROE improvement

- **Focus on SPE business**
- **Leverage product line up and respond to diversifying needs**
- **New framework and executive structure to enhance our strengths**

Financial Model, Shareholder Returns Policy

Tetsuro Hori

Corporate Director, Senior Vice President & General Manager

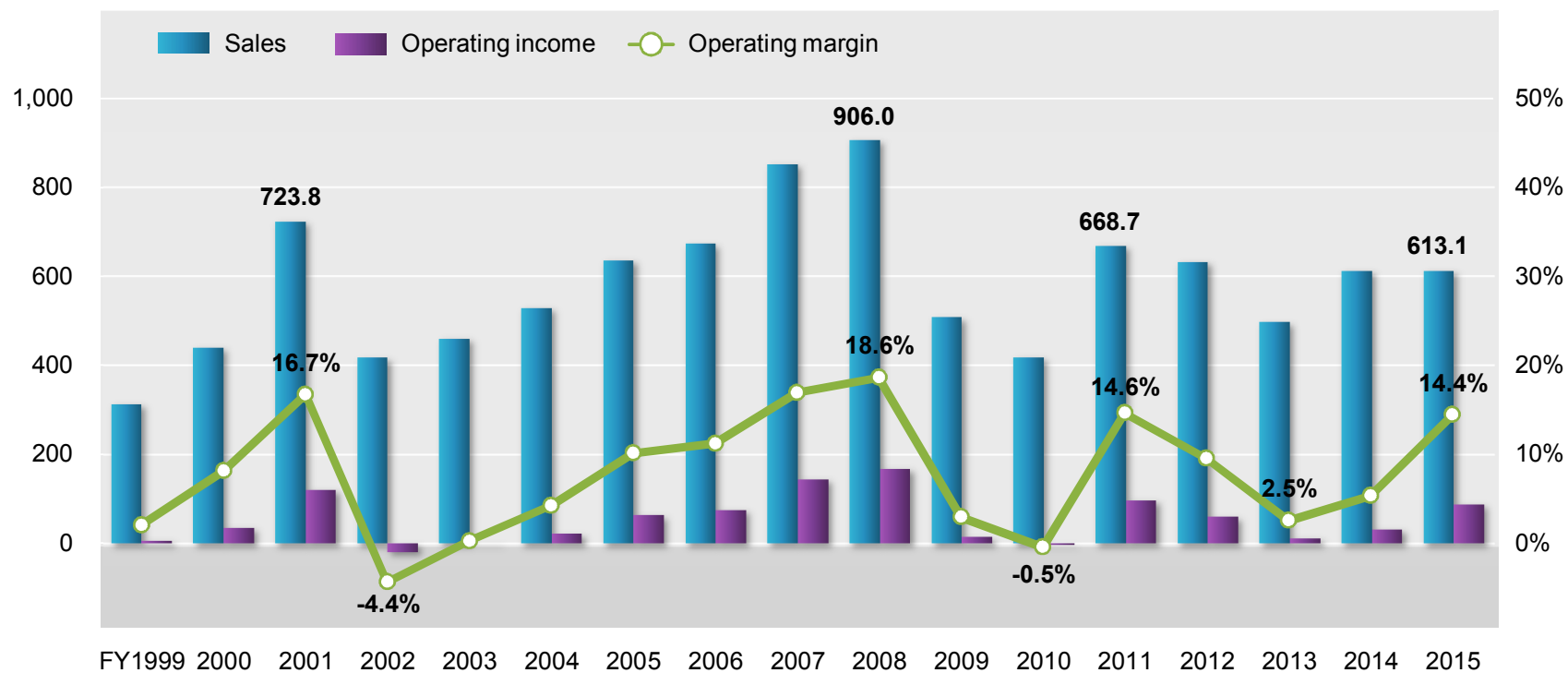
July 10 , 2015



TOKYO ELECTRON

Financial Performance

(Billion Yen)



Financial Model (toward FY2020)

- Build an earnings structure capable of attaining an OPM of 25% at WFE market size \$37B (Billion Yen)

	FY2016 (Estimate)	FY2020 (Medium-term plan)	
	WFE \$33.5B	WFE \$30B	WFE \$37B
Net sales	675	720	900
SPE	625	660	840
FPD	47	60	60
Gross profit	265	305	395
Gross profit margin	39%	42%	44%
SG&A expenses	153	160	170
SG&A expense ratio	23%	22%	19%
Operating income	112	145	225
Operating margin	17%	20%	25%
Net income	79	100	155

The semiconductor production process can be divided into two sequential sub-processes referred to as front-end (wafer fabrication) and back-end (assembly and test) production. WFE (wafer fabrication equipment) is used in the front-end production process.

SPE Sales (WFE \$37B)

➤ Sales growth in excess of market growth

(Billion Yen)

	FY2016 (Estimate)	FY2020 (Medium-term plan)	Growth
	WFE \$33.5B	WFE \$37B	WFE +10%
Sales	625	840	+34%
New equipment	465	650	+40%
Field solutions	160	190	+19%

- Enhance our ability to identify the technological needs of our customers and to develop products to meet them
- Respond to growing demand for field solutions

FPD Sales

- Target sales growth in leading-edge areas, where we can differentiate our technology

(Billion Yen)

	FY2016 (Estimate)	FY2020 (Medium-term plan)	Growth
Sales	47	60	+28%
New equipment	38	48	+26%
Field solutions	9	12	+33%

- Focus on etching systems and OLED deposition systems, areas in which we have technological superiority

Gross Profit (WFE \$37B)

➤ Gross profit margin: up 5%pts

(Billion Yen)

	FY2016 (Estimate)	FY2020 (Medium-term plan)	Growth
Gross profit	265	395	+49%
Gross profit margin	39%	44%	+5%pts

- Raise marginal profit ratio through efforts to enhance product competitiveness
- Expand field solutions business
- Reduce costs by sharing technology across our products
- Reduce costs, shorten production lead-times and pursue quality from the design stage onward

SG&A Expenses (WFE \$37B)

- SG&A expense ratio: improve by 4%pts

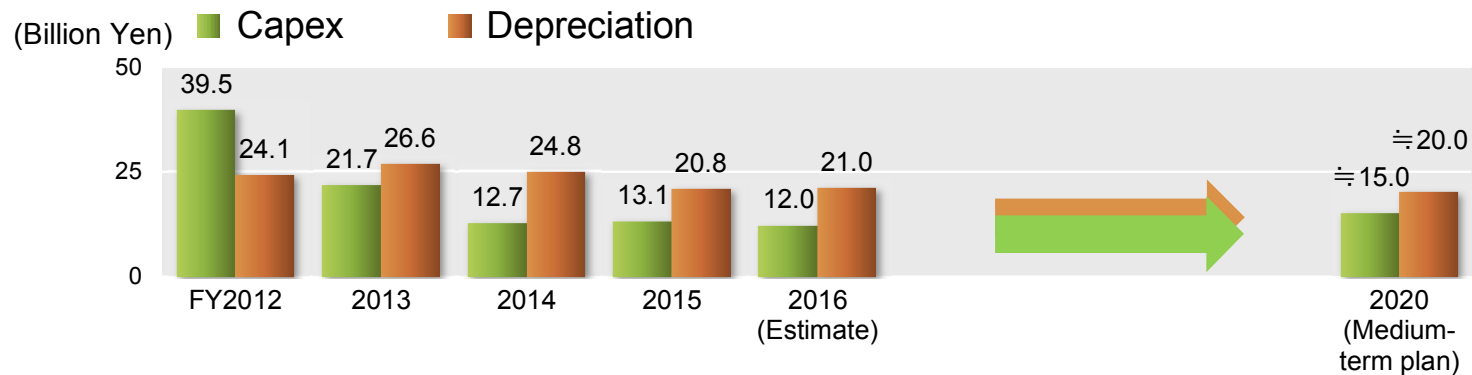
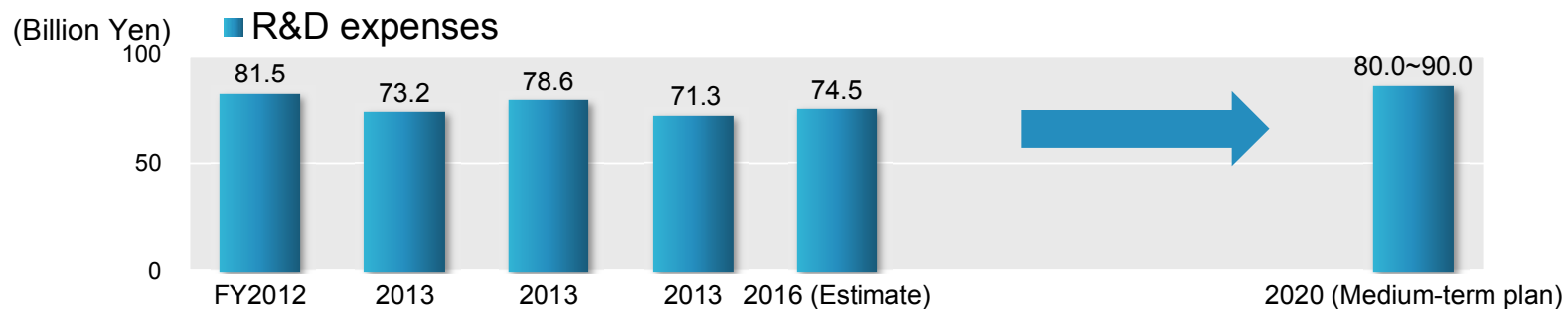
(Billion Yen)

	FY2016 (Estimate)	FY2020 (Medium-term plan)	Growth
SG&A expenses	153	170	+11%
SG&A expense ratio	23%	19%	-4%pts

- Pursue operational efficiencies by reinforcing regional sales & marketing and field engineering capabilities under account management structure
- Select development projects carefully, focusing on SPE

R&D Expense, Capex Plans

- Advance developmental efforts that are necessary for growth while working to improve their efficiency
- Maintain capex at around its current level



Managerial Targets

- We target a global level of profitability

WFE Market	\$30B	\$37B
Operating margin	20%	25%
ROE	15%	20%

The semiconductor production process can be divided into two sequential sub-processes referred to as front-end (wafer fabrication) and back-end (assembly and test) production. WFE (wafer fabrication equipment) is used in the front-end production process.

Capital Policy, Shareholder Returns

➤ Approach to capital policy

- While closely monitoring the business environment and our necessary cash balance, we will strive to raise ROE through earnings maximization and asset turnover improvement to efficiently utilize shareholders equity

➤ Approach to shareholder returns

- Business trends in our industry can be volatile and our policy is to link dividend payments to business performance
- However, to assure stable returns to our shareholders, we will utilize our sound financial foundation to establish a minimum DPS payment

New Policy for Shareholder Returns

Dividend payout ratio: 50%

Annual DPS of not less than ¥150

We will review our dividend policy if the company does not generate net income for two consecutive fiscal years

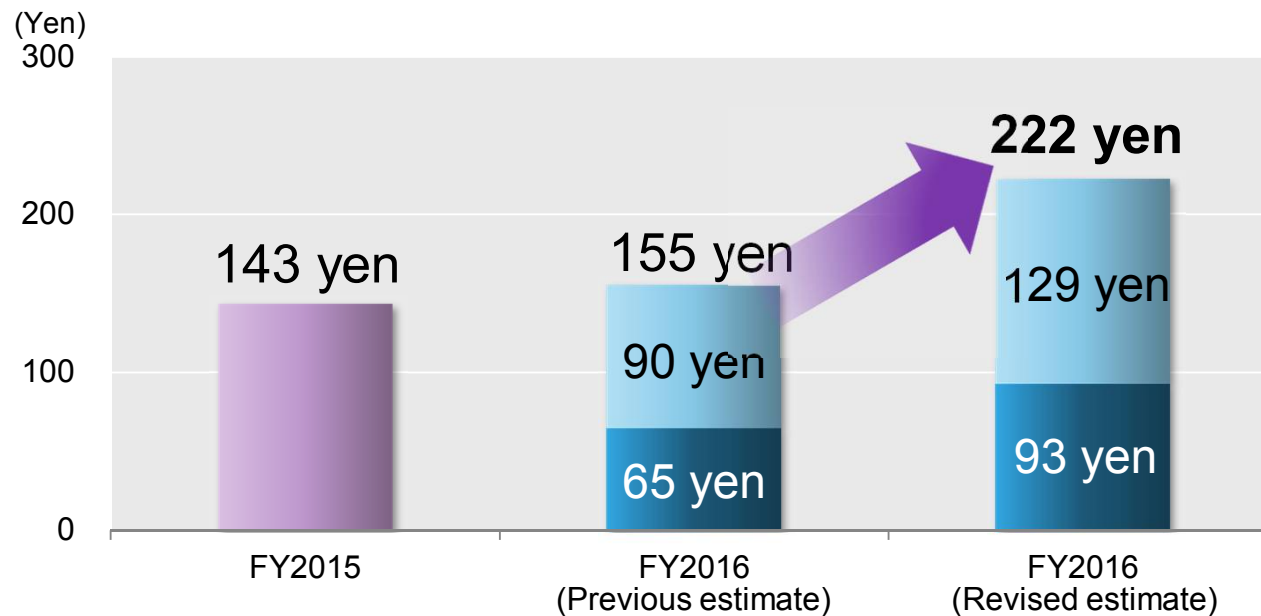
We will flexibly consider share buybacks

Our previous dividend policy since FY2011 year-end dividend was performance-linked payout ratio of around 35%.

FY2016 Dividend Forecast (Announced on July 10, 2015)

- Revised dividend forecast based on new shareholder returns policy

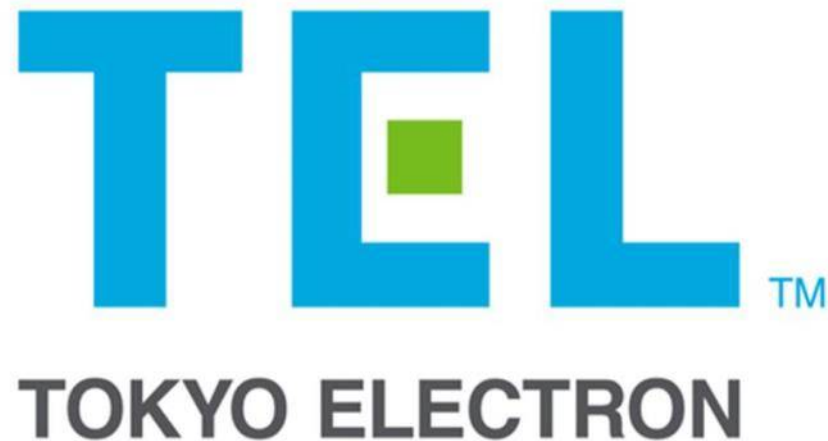
Dividend per share (Estimate)		
Interim	Year-end	Year Total
93 yen	129 yen	222 yen



Summary

We strive to outperform market growth and enhance our corporate value

New Corporate Logo



▶ **Disclaimer regarding forward-looking statement**

Forecast of TEL's performance and future prospects and other sort of information published are made based on information available at the time of publication. Actual performance and results may differ significantly from the forecast described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD/PV market conditions, intensification of sales competition, safety and product quality management, and intellectual property-related risks.

▶ **Processing of numbers**

For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

▶ **Exchange Risk**

In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD/PV panel production equipment are denominated in yen. While some settlements are denominated in dollars, exchange risk is hedged as forward exchange contracts are made individually at the time of booking. Accordingly, the effect of exchange rates on profits is negligible.

FPD/PV: Flat panel display/Photovoltaic